What is claimed is:

1. A random number generator comprising:

a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a count value of the clock signal with respect to a transition of the random signal; and

a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to provide a first random number signal.

2. The random number generator of claim 1, wherein the random signal manifests a characteristic in which power spectrum intensity varies with an increase of frequency.

3. The random number generator of claim 1, wherein the random signal manifests a characteristic in which power spectrum intensity decreases with an increase of frequency.

4. The random number generator of claim 1, further comprising a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal.

5. The random number generator of claim 4, wherein the frequency of the random number acquisition clock is lower than the frequency of the random signal.

6. The random number generator of claim 4, wherein the transition of the random number acquisition clock signal represents a leading edge of the random number acquisition clock signal when the random number acquisition clock signal changes from a low level to a high level.

7. The random number generator of claim 1, wherein a pulse counter is accessible by the clock enable input, and the output of the pulse counter becomes the random signal.

8. The random number generator of claim 1, further comprising an inverter connected between the clock enable input side and a clock input side of the first latch circuit.

9. The random number generator of claim 1, wherein a period of the clock signal is less than a half of a on-state zone Tz which is obtained by subtracting a minimum on-state pulse width Tmin from a maximum on-state pulse width Tmax.

10. The random number generator of claim 1, wherein the first latch circuit is a D type flip-flop.

11. A random number generator comprising:

an AND circuit configured to be supplied with a random signal and a clock signal, and to generate a logic product of the random signal and the clock signal;

a dividing latch circuit configured to provide alternately a high level signal and a low level signal with respect to the logic product output; and

a first latch circuit configured to latch the count value with respect to a transition of the random signal, and to provide a random number signal.

12. The random number generator of claim 11, wherein the random signal manifests a characteristic in which power spectrum intensity varies with an increase of frequency.

13. The random number generator of claim 11, wherein the random signal manifests a characteristic in which power spectrum intensity decreases with an increase of frequency.

14. The random number generator of claim 11, further comprising a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal.

15. The random number generator of claim 14, wherein the frequency of the random number acquisition clock is lower than the frequency of the random signal.

16. The random number generator of claim 14, wherein the transition of the random number acquisition clock signal represents a leading edge of the random number acquisition clock signal when the random number acquisition clock signal changes from a low level to a high level.

17. The random number generator of claim 11, further comprising a pulse counter being accessible by the clock enable input, wherein the output of the pulse counter becomes the random signal.

18. The random number generator of claim 11, wherein a period of the clock signal is less than a half of a on-state zone Tz which is obtained by subtracting a minimum on-state pulse width Tmin from a maximum on-state pulse width Tmax.

19. The random number generator of claim 11, further comprising an inverter connected between the first input side and a clock input side of the first latch circuit.

20. The random number generator of claim 11, wherein the first latch circuit is a J-K type flip-flop.